MATH FOR PHYSICS

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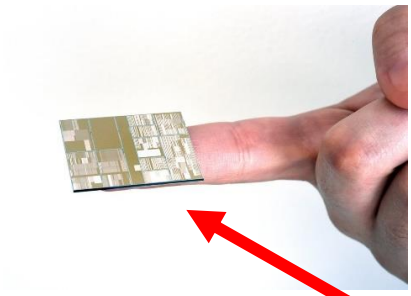
IBM Discloses Working Version of a Much Higher-Capacity Chip



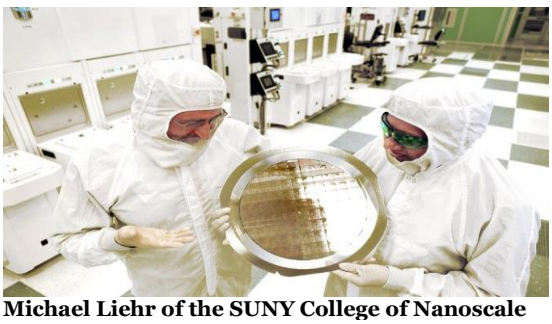
INTRODUCTION: **Generations of computer chips reduce each generation by ~ 50 % in circuit area. Purpose of this application is to verify that each generation of chip area reduces ~ 50 % . As seen below the three present generations are: L = 14 nm, 10 nm, 7 nm. Let L = length and width of a square chip. Thus, $A = L^2$.**

QUESTIONS: **Show area of chip is reduced ~ 50% with each new generation of chip…. …..14nm to 10 nm, 10 nm to 7 nm**

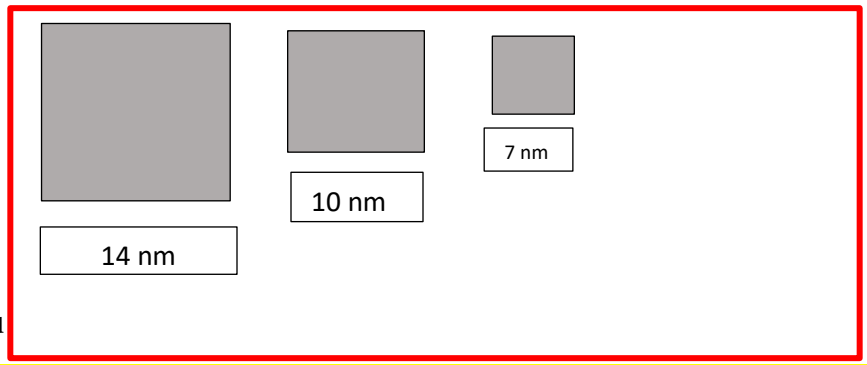
HINTS: **Area = $A = L^2$, nm = nanometer = 10^{-9} meter, see sketch of chipsize below.**

A **working sample of a chip with seven-nanometer transistors**. IBM said it made the advance by **using silicon-germanium instead of pure silicon.**

IBM said on Thursday that it had made working versions of **ultradense computer chips**, with roughly four times the capacity of today's most powerful chips. The announcement, made on behalf of an international consortium led by IBM, the giant computer company, is part of an effort to manufacture the most advanced computer chips in New York's Hudson Valley, where IBM is investing $3 billion in a private-public partnership with New York State, GlobalFoundries, Samsung and equipment vendors. The development lifts a bit of the cloud that has fallen over the semiconductor industry, which has struggled to maintain its legendary pace of **doubling transistor density every two years.** Intel, which for decades has been the industry leader, has faced technical challenges in recent years. Moreover, technologists have begun to question whether the longstanding pace of chip improvement, known as **Moore's Law, would continue past the current 14-nanometer generation of chips.** Each generation of chip technology is defined by the minimum size of fundamental components that switch current at nanosecond intervals. **Today the industry is making the commercial transition from what the industry generally describes as(((14-nanometer manufacturing to 10-nanometer manufacturing.)))Each generation brings roughly a 50 percent reduction in the area required by a given amount of circuitry.**



Michael Liehr of the SUNY College of Nanoscale Science and Engineering, left, and Bala Haranand of IBM examine a wafer comprised of the new chips.



The company said on Thursday that it had **working samples of chips with seven-nanometer transistors**. It made the research advance by using **silicon-germanium** instead of pure silicon in key regions of the molecular-size switches. It must also grapple with the shift to using extreme ultraviolet, or EUV, light to etch patterns on chips at a resolution that approaches the diameter of individual atoms. In the past, **Intel said it could see its way toward seven-nanometer manufacturing. But it has not said when that generation of chip making might arrive.**

Ultimately the goal is to create circuits that have been reduced in area by another 50 percent over the industry's 10-nanometer technology generation scheduled to be introduced next year.